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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,181	07/19/2001	Paul A. Farrar	MICRON.170A	9085

20995 7590 03/29/2004

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,181	PAUL A. FARRAR	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

1. In view of the appeal brief filed on December 19, 2003, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Objections

2. Claim 1 is objected to because of the following informalities: line 8, "a" [sic: an]. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 7 and 9 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art in view of Farrar '792.

Regarding claims 1, 2 and 19, the acknowledged prior art discloses in e.g., pages 1 – 3 a high density semiconductor structure having a plurality of integrated circuit chips, comprising:

- a first integrated circuit chip (first semiconductor chip from the multichip cube structures) having an upper bonding surface;
- a second integrated circuit chip (second semiconductor chip from the multichip cube structures) secured to the first chip in a manner such that a lower bonding surface of the second chip is positioned adjacent to the upper bonding surface of the first chip; and
- a first or chip insulating layer (a part of the insulator in the prior art constitutes as the chip insulating layer; claim 1 and claim 19) disposed between the first and second chips, so as to provide electrical isolation between the chips, wherein the chip insulating layer comprises an insulating material; and
- a second or conductor insulating layer (a part of the insulator in the prior art constitutes as the conductor insulating layer; claim 2 and claim 19) formed on the upper bonding surface of the first chip, wherein the conductor insulating layer provides electrical isolation between adjacent conductive leads (conductive leads) disposed on the upper bonding surface of the first chip, wherein the conductor insulating layer comprises an insulating material.

The acknowledged prior art does not disclose a plurality of enclosed regions of air dispersed within and throughout the insulating material of the chip or first and conductor or second insulating layer wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. However, Farrar teaches in e.g., Fig. 1B and column 8, lines 39 – 62 a plurality of enclosed regions of air (cells) dispersed within and throughout an insulating material of an insulating layer (116, foamed polyimide layer) wherein the dielectric constant of the chip insulating layer is less than the dielectric constant of the insulating material. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify the acknowledged prior art by substituting the known insulator layers with the foamed polyimide layers which has the plurality of enclosed regions of air as taught by Farrar. The ordinary artisan would have been motivated to modify the acknowledged prior art in the manner described above for at least the purpose of (1) providing an integrated circuit that has adequate mechanical integrity, as well as a relatively low dielectric constant (column 2, lines 33 – 34) thereby further decreasing the capacitive coupling between adjacent leads of a multichip structure, a goal that Applicant acknowledges was previously known, (2) decreasing RC delay and (3) enhancing the operating rate of devices.

Regarding claims 3 and 4, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the chip insulating layer comprising a foamed polymeric material.

Regarding claim 5, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the foamed polymeric material comprising a foamed polyimide (116).

Regarding claim 6, Farrar discloses that the foamed polyimide may be formed to a thickness within the range of 0.2 to 10 microns depending upon the particular application and

that for many applications a thickness of 2.1 microns provides adequate electrical isolation (column 6, lines 53 – 65).

Regarding claim 7, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the foamed polymeric material comprising a hydrophobic material wherein the hydrophobic material is treated so as to provide the material with hydrophilic properties.

Regarding claims 9 and 10, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 each enclosed region of air being "approximately" 0.1 micron.

Regarding claim 11, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 each enclosed region of air being less than the minimum distance separating adjacent conductive leads.

Regarding claim 12, Farrar discloses in e.g., Fig. 1B and column 2, lines 8 – 16 the dielectric constant of the chip insulating layer (foamed layer has a dielectric constants 1.2 – 1.8) being "approximately" one third of the dielectric constant of the insulating material (non-foamed layer has a dielectric constants 2.8 – 3.5).

Regarding claim 13, Farrar discloses in e.g., Fig. 1B and column 2, lines 14 – 16 the dielectric constant of the insulating layer being less than 1.5.

Regarding claim 14, the acknowledged prior art discloses that the conductive leads may be made of an aluminum alloy (page 1, line 20).

Regarding claim 15, the acknowledged prior art discloses in e.g., pages 1 – 3 a third integrated circuit chip (third semiconductor chip from the multichip cube structures) wherein the third chip is secured to the second chip in a manner such that a lower surface of the third chip is

positioned adjacent an upper surface of the second chip wherein a third insulating layer (the third insulator in the prior art) is disposed between the second and third chips.

Regarding claims 16 and 18, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the third insulating layer comprising a foamed polymeric material.

Regarding claim 17, the acknowledged prior art discloses in e.g., pages 1 – 3 the first integrated circuit chip further comprising a lower surface wherein a fourth insulating layer (the fourth insulator in the prior art) is formed on the lower surface of the first chip.

Regarding claim 20, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the first insulation material comprising a polymeric material.

Regarding claim 21, the limitation "the polymeric material is treated with a supercritical fluid so as to produce the enclosed regions of the air in the material" is product-by-process claim, even though product-by-process claim is limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process. In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985) (citations omitted). A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, **190 USPQ 15 at 17** (footnote 3). See also In re Brown, **173 USPQ 685**: In re Luck, **177 USPQ 523**; In re Fessmann, **180 USPQ 324**: In re Avery, **186 USPQ 116**; In re Wertheim, **191 USPQ 90 (209 USPQ 254** does not deal with this issue); and In re Marosi et al., **218 USPQ 289** final product per se which must be determined in a "product by, all of" claim, and not the patentability of the process, and that an old or obvious product, whether claimed in "product by

process" claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Regarding claim 22, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 each enclosed region of air being less than the distance between adjacent metal leads on the upper surface of the first chip.

Regarding claim 23, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the second insulating material comprising a polymeric material.

Regarding claim 24, Farrar discloses in e.g., Fig. 1B and column 8, lines 39 – 62 the polymeric material being polyimide.

Allowable Subject Matter

5. Claims 8, 25 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8 and 25 contain allowable subject matter because none of references of record teach or suggest, either singularly or in combination, at least the limitation of a foamed polymeric material encompassing polynorbornene.

Since claim 26 is a dependent claim of objected claim (claim 25), this claim is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (e.g., claim 25).

Response to Arguments

6. Applicant's arguments with respect to claims 1 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. DiStefano et al. '681 discloses a foamed polyimide layer may be employed as an insulating layer between a semiconductor chip and an underlying substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRADLEY BAUMEISTER
PRIMARY EXAMINER

c.c.
March 22, 2004